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WORKING GROUP B (MICROELECTRONICS)

DoD SILICON INVESTMENT STRATEGY

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PREFACE

The billion dollar Very High Speed Integrated Circuits (VHSIC) program of the 1980s absorbed virtually all of DoD's silicon-based research and development resources during that period. With the ending of VHSIC, DoD support of this essential core technology ceased with the exception of the highly targeted programs of DARPA. While the use of commercial silicon devices in defense equipment continues to increase, DoD investments that bias this commercial technology for defense purposes do not exist, nor are the unique military application areas being adequately addressed. Furthermore, the commercial technology base upon which DoD has become highly dependent has become increasingly short-term because of competitive pressures.

This report urges restoration of support for the mainstream silicon technology base to at least pre-VHSIC levels. It further urges that this support be effectively managed through a "Silicon Investment Strategy" aimed at filling in gaps in commercially funded R&D efforts, particularly with respect to long-range research, and, to the fullest extent possible, leveraging the much larger commercial investment in this area of technology. Changes now under way both in commercial semiconductor R&D and in the DoD technology structure will increase the effectiveness of these investments, if accomplished expeditiously, and will enable a strong response to present and future military technology needs.

The conclusions and recommendations reported here were developed by DoD's Advisory Group on Electron Devices—specifically by AGED's Working Group B, which is responsible for coordinating microelectronic device development for DoD. Formal consideration of the relevant issues—obvious steady erosion of the silicon tech base, the need for an effective investment strategy, etc.—began on 13 December 1990 with the holding of a "Special Technology Area Review" and continued in a series of meetings held throughout 1991. This report and the "Silicon Investment Strategy" it proposes are the culmination of those deliberations.

On behalf of Working Group B, I would like to take this opportunity to express my sincere appreciation to all the participants—identified on the next page—for their valuable contribution to this study. This applies particularly to Dr. Robert Burger of SRC, principal author of the overall report, and to Dr. John M. MacCallum, Jr., ODDDR&E/ET, whose support and encouragement were essential to this effort. Finally, I would like to thank Mr. Jack Kilby, AGED Chairman, for his insightful comments and warm endorsement.

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FOREWORD

This country's once-significant lead in silicon integrated circuit technology, both commercial and military, has diminished considerably. In some areas, it has disappeared entirely. This trend cannot be allowed to continue, given the key role of integrated circuits in advancing the performance of almost all military systems.

It is impossible for DoD, by itself, to reverse this trend. However, by using its funding effectively and working closely with commercial industry development efforts, DoD can have a large impact on the competitive status of the U.S. industry and influence it to better serve military system needs. DoD has already entered into a new era of tri-Service and government-industry cooperative activities in the development and acquisition of electronic components. Through partnerships, consortia and other teaming arrangements, DoD can and should leverage its limited resources to advance the silicon technology base upon which it relies. The accomplishment of this requires a coherent strategy such as that proposed in this report.

This report emphasizes the new synergisms with commercial technology required to advance military capabilities and the need for an investment strategy to make the best use of DoD resources.

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EXECUTIVE SUMMARY

In view of the central importance of silicon integrated circuits in defense electronics and pervasive changes now under way within DoD and the defense supplier base, the Working Group concludes that all but a small fraction of DoD's silicon integrated circuit needs should be obtained from commercial sources and that DoD's silicon integrated circuit R&D should be harmonized with that of the private sector. Accomplishing these ends will require a focused management strategy dedicated to a major modernization of the acquisition system in this area.

Silicon integrated circuit technology has emerged as one of the most essential of the core technologies in the U.S. military arsenal. The performance advantage offered by this technology has led to its pervasive use in the electronics of practically every U.S. military system and has accounted for much of the success of the nation's force multiplication strategy—the ability of a small, technologically superior U.S. force to decisively defeat a much larger enemy.

In recent years, however, the once-formidable U.S. superiority in silicon-based integrated circuit technology has all but vanished in a number of militarily critical areas—the result of sharply declining R&D investment, the loss of a number of related high-volume commercial markets, and the skyrocketing cost of merely staying competitive in this field. *(Do not be misled by the stunning success of U.S. weaponry during Desert Storm: Much of that success came from electronics developed during the 1960s and 1970s, when the U.S. was still clearly the world leader in integrated circuit technology.)* But even in those areas where the U.S. integrated circuit industry continues to be strong, the silicon device technology used in U.S. defense systems is years behind internationally available commercial technology—the result of lengthy system development cycles and life cycles, outmoded procurement practices, and generally unsuccessful attempts to provide unique capabilities for defense systems through use of non-mainstream technologies.

In these times of rapidly changing defense structures and threats, it is essential that the U.S. continue to present a credible deterrent to would-be aggressors. A strong military electronics capability based on world-class silicon integrated circuit technology can provide that deterrence—and, if need be, a flexible and effective response to any aggressive act.

At present, DoD investments are not adequately addressing this critical issue and, with decreasing resources available, will not correct the problem unless a radically different silicon device investment strategy is defined and implemented. Such a strategy is proposed in this report.

The fundamental tenets of a silicon investment strategy for DoD are as follows:

- Silicon integrated circuit technology provides, and will provide for the foreseeable future, the core performance determinant of defense electronics. Performance enhancements derived from other semiconductors or other component technologies will provide only limited advantages without superior silicon integrated circuits.

- It has been amply demonstrated that the commercial industry drives the performance growth of integrated circuits and that is not possible to produce special integrated circuits for defense purposes that are equal to the commercial state of the art in terms of quality, reliability, performance and cost. Since defense integrated circuits are effectively products of commercial fabrication technology, U.S. defense electronics capabilities are closely correlated with the capabilities and robustness of U.S. industry.

- The U.S. semiconductor industry lags foreign producers in several areas. Manufacturing is a noteworthy example. As a result, some of the most advanced integrated circuit technologies are now readily available to all nations for incorporation in defense systems, seriously threatening future U.S. weapons superiority.

The objective of a DoD Silicon Investment Strategy is to provide silicon integrated circuits for U.S. defense systems that will enable the electronics in those systems to outperform the military electronic capabilities of any potential adversary. In light of present circumstances and trends, effective accomplishment of that objective will require adoption of a number of brand-new policies and special management methods, such as:

- Establish as DoD policy that all silicon integrated circuits and other silicon/semiconductor devices used in defense systems be procured from commercial U.S. production unless there exists a specific clear and compelling performance requirement that cannot be met from commercial production. In those unique cases, performance enhancements of commercial devices will be undertaken.

- Phase out facilities, procurement requirements, and R&D that exists to support an independent defense supply base of silicon integrated circuits except for clearly defined efforts associated with meeting the small number of unique DoD needs. (The NSA IC facility and limited radiation hardening programs are clearly meeting unique DoD needs.) Also merge separate industry and DoD specifications and standards.

- Redirect DoD resources to: (1) establish U.S. leadership in silicon integrated circuit technology through cooperative R&D with industry, (2) encourage commercial developments to move in directions that are in closer alignment with DoD special needs, and (3) meet the limited number of special military requirements that cannot be met by present commercial lines.

- Apply resources for these purposes that are consistent with the importance of the technology, the urgency of the need, and the size of the overall DoD budget.

- Establish a DoD program that responds to the technology needs of all of DoD, and maintain a DoD silicon technology road map that has a seamless interface with U.S. industrial technology, optimizes DoD technology investments, and transfers technology from all sources to DoD users.

Note that JDL Project Reliance—specifically the tri-Service Technology Panel for Electronic Devices—would be an effective advisory/oversight group for aiding the implementation of the required Silicon Device Investment Strategy, or at least provide a base from which that strategy could be implemented.

The body of this report provides a basis for these recommendations. The specific issues addressed in each section of the report are indicated below:

I. INTRODUCTION - Discusses status and importance of silicon technology and role of DoD, and introduces a strategy.

II. BACKGROUND - Provides history and present concerns.

III. DEFENSE RELEVANCE OF SILICON TECHNOLOGY - Discusses general DoD requirements and specific DoD applications and implications of foreign dependence.

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I. INTRODUCTION

Silicon device technology is an absolutely essential and pervasive enabler of defense operations and systems. However, DoD is not participating sufficiently in the advancement of this technology to assure a continued U.S. advantage in defense electronics, nor is it applying the available technology products effectively.

If current trends continue, U.S. technology will be unable to provide future military systems with the force multiplier advantage that exists in today's systems.

> *It is recognized that even when advanced silicon technology is available to other countries, they may have even greater difficulty than the U.S. in assimilating the technology into defense systems either because their access to the technology is limited, their system capabilities are inadequate, or their bureaucracy cannot respond effectively. Still, a determined adversary can overcome these barriers. Consequently, preservation of this nation's long-standing force multiplier advantage requires that U.S. capabilities in the key area of silicon device technology be equal to or better than that available in world commercial markets.*

Desert Storm demonstrated the importance of defense electronics to the U.S. military. With reduced military force levels, electronics superiority becomes even more important. Electronics superiority requires leadership in silicon technology. The U.S. is in the process of losing its former leadership in silicon technology and, thus, its defense electronics advantage.

With respect to defining, designing, and developing electronic systems employing silicon integrated circuits (ICs), the U.S. currently has a distinct advantage. In the future, with much more of the system performance built into each silicon chip, system capabilities alone will no longer provide the required electronic technology edge. Superior silicon chip technology is a necessity. The U.S. now lags in important manufacturing, materials and packaging technologies for silicon ICs and its leadership in integrated circuit design is threatened.

One must not be misled by the outstanding success of technology in Desert Storm. This success is a legacy of a previous era when U.S. leadership in semiconductors and other technologies was clear.

For systems being developed today, different conditions apply. U.S. technology is not the unquestioned best, so system designers must either use foreign technology or settle for less than the best components. If present trends continue, future U.S. systems built with U.S. components will be outperformed by systems using foreign-sourced components.

Separate production facilities for semiconductor components used in defense systems no longer exist in this country. Almost all ICs and other semiconductor components used in DoD applications are either commercial devices or commercial devices with superficial production, packaging, and testing changes. The impact of these relatively minor changes and the accompanying defense procurement paperwork burden serve to increase substantially the cost of "qualified" devices to the DoD and to

delay their insertion into defense systems. It is debatable whether these "qualified" components are superior to their commercial counterparts. Often they lag commercial parts in both performance and quality by more than one technology generation.

More important than cost is the dependence of defense semiconductor technology on capabilities that can only be established in high-volume commercial production. The attainment of competitive performance, quality, and reliability requires that defense devices be obtained from commercial high-volume production lines operating at the leading edge of the technology. Because the competitive position of the U.S. semiconductor industry is declining, there is no assurance that domestic leading-edge production facilities will continue to be available in the future. Although some offshore acquisition of defense components is reasonable, becoming dependent upon foreign suppliers for the key technologies and components that are the enablers for critical systems carries unacceptable risk and is inconsistent with U.S. defense policy.

U.S. industry production of semiconductor devices exceeds $30 billion/year. Something less than $1 billion of this total involves devices made from semiconductor materials other than silicon. DoD buys about $3 billion worth of semiconductors each year, mostly embedded in military systems and other electronic products such as workstations, telephone switches, engine controls, and bar-code readers.

The argument has been made that with such a small share of the semiconductor market, the DoD cannot influence the direction of the industry. That may be true, particularly if the defense and commercial markets are perceived as divergent. However, when viewing military and commercial integrated circuits as one market and taking note of the increasingly short-term objectives of industrial R&D investments, DoD technology investments can exert much influence on the pace and thrust of development and on long-range goals.

Because of delays in system development and deployment and because of compartmentalization of responsibilities, DoD systems are characteristically late users of new integrated circuit technology. While programs have been initiated to support fielded systems, much of DoD's semiconductor technology funds are spent to assure lifetime supplies of spare parts—often obsolete integrated circuits.

DoD should seek to be an important purchaser of leading-edge high-performance products instead of being a relatively small purchaser of commodity parts or of trying to maintain supplies of low-performance, obsolete devices. There is a direct relationship between the capabilities of the domestic semiconductor industry and defense electronics. Stated succinctly, defense electronics superiority requires a globally superior commercial silicon IC technology base.

In the U.S., commercial semiconductor companies have been reluctant to address the relatively small market represented by national defense because of the perception that it absorbs talent and resources from the commercial products on which these companies depend for survival. DoD requirements have caused industry to create expensive defense-product-only facilities that are inadequately coupled to commercial production counterparts and reflect the shortcomings already discussed. The effect of this separation is to produce silicon IC obsolescence in weapons systems. Viewing the two markets as one and concentrating available resources onto that one market would help ensure silicon IC leadership for both commerce and defense.

This report contends that with an appropriate strategy and careful management of even reduced resources, the DoD can change present trends and, in the process, obtain and maintain a technology advantage in future U.S. defense systems.

An appropriate investment strategy is one that would redirect resources now used for proprietary defense R&D and acquisition and maintenance of dedicated defense production of semiconductors to one that would:

1. Apply the advanced technology capabilities of the U.S. commercial integrated circuit industry to the full advantage of defense electronics, and

2. Provide the U.S. semiconductor industry with R&D and application leadership promotive of sustaining technology and manufacturing leadership, thereby enabling that industry to better serve defense needs.

By advancing technology with well-chosen R&D investments in directions defined by defense needs, while at the same time taking advantage of the high-volume learning curves of industry, DoD would succeed in obtaining the capabilities needed for future military systems.

To accomplish this redirection and to ensure silicon technology leadership, DoD should develop a silicon device strategy that guides its investments in the most effective manner and maintains them at the proper level relative to other DoD technology investments. Specifically, this strategy should encompass:

1. Development and maintenance of a DoD silicon technology road map that has a seamless interface with U.S. industrial technology,

2. Optimization of DoD silicon technology investments,

3. Transfer of technology to DoD users, and

4. Definition of appropriate investment levels within the overall context of DoD technology budgets.

This silicon-device-focused program would ensure that the U.S. military possesses the technology it will need to perform as well in the "Desert Storms" of the next century as it performed in Desert Storm-1991.

II. BACKGROUND

In a 1966 review of early integrated circuit developments, General B. Schriever stated that, "The birth and explosive growth of integrated circuits can be directly attributed to ... wise policy direction by the Department of Defense..."[1] The nurturing of this technology from its 1958 invention through the early 1960s by the DoD was spurred by well-defined operational requirements for integrated circuits. The operational importance of silicon integrated circuits to defense is even greater now than it was three decades ago, but the nurturing of the technology was ceded to the industry when commercial markets began their rapid growth in the late 1960s.

Semiconductor materials and microelectronics are critically important and appropriately lead the list of critical defense technologies.[2] Silicon integrated circuits comprise the largest share of the semiconductors used by defense. This is recognized by DoD's annual investment of over $300 million dollars of 6.1, 6.2, and 6.3a funds for silicon integrated device technology for defense applications.

As indicated in Table 1, the Department of Defense was the driving force that caused the integrated circuit to become a reality in the period from 1958 to 1964. The initial and, at that time, sizable efforts to create the technology and demonstrate its reality were a DoD initiative. Without the impetus of the early R&D contracts, the development of the integrated circuit would not have occurred when it did. The momentum created by the early and rapid demonstration of the reality of the IC in the Minuteman computer led to the creation of a rapid-growth industry in just a few years.

Commercialization of the silicon IC in computers, telecommunications, and consumer electronics, however, eventually outpaced DoD's ability to assimilate the products into its systems. The result was that over the next 15 years, DoD gradually became a customer for the commercial technology but contributed only peripherally to its advancement.

In 1980, recognizing that the technology being applied in defense systems was generations behind that being applied in commercial products, DoD established a major program to address this issue. The 10-year VHSIC (Very High Speed Integrated Circuit) program sought to expedite the incorporation of advanced silicon IC technology into defense systems. VHSIC not only achieved that objective but had an important impact on the progress of the commercial industry. Indeed, "... most experts agree that without VHSIC, semiconductor development in the U.S. wouldn't have progressed so quickly toward submicron geometries, even in the commercial world."[3]

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[1] General B.A. Schriever, Commander, Air Force Systems Command, in Integrated Circuits Come of Age, Air Force Systems Command, USAF, Washington, D.C., 1966.

[2] U.S. Department of Defense, Critical Technologies Plan, May 1991.

[3] Electronics, June 1989, p. 97.

VHSIC was not intended to address the broader needs associated with U.S. integrated circuit capabilities; instead, it was focused on speeding insertion of those capabilities into defense systems. During the course of VHSIC, U.S. integrated circuit technology lost ground to other nations as a result of the targeting tactics of foreign industries, supported closely by investments and protective measures of governments that recognized the strategic commercial importance of that technology. While VHSIC provided a focused thrust in silicon integrated circuit technology development and insertion, it had the effect of curtailing silicon investments by the Service organizations. Thus, at the conclusion of VHSIC, silicon R&D activity was essentially nonexistent, insofar as DoD was concerned.

In 1987, the major vulnerability of the U.S. in semiconductor technology was identified as its lag in developing and applying the complex manufacturing techniques and technologies required for producing advanced integrated circuits.[4] The response was a DoD/industry cooperative effort aimed at restoring the U.S. competitiveness in silicon integrated circuit manufacturing technology. This program, SEMATECH, has proven to be a highly successful paradigm for focusing required resources upon a need shared by defense and industry.[5]

Table 1. SIGNIFICANT MILESTONES IN DoD MICROELECTRONICS

1958	Molecular electronics
1959	Integrated circuits R&D
1960	IC production contracts
1961	IC computer demonstration
1964	Flight-test of Minuteman computer, IC market reaches $40 million
1965	VLSI demonstrations initiated, Low light level CCD
1970-80	Limited Service investments in silicon technology, Research focus on esoteric semiconductors
1980-89	VHSIC Program
1987-92	SEMATECH

[4] Report of the Defense Science Board Task Force on Defense Semiconductor Dependency, Feb. 1987, Office of the Undersecretary of Defense for Acquisition, Washington, D.C. 20301.

[5] SEMATECH, 1991 Update, March 4, 1991.

Concerns within DoD now relate to silicon technology and its defense applications, including:

1. Availability of leading-edge silicon device technology for U.S. defense systems—technology that will give future sustems the same force multiplier advantage that current systems possess.

2. Assured sources for system-critical devices required to make and maintain current operating systems.

3. Maintenance of a knowledge base of high-payoff device research areas and directions, needed for the planning of advanced defense systems.

4. Security of highly sensitive knowledge embedded in mask patterns for integrated circuit manufacture, especially if it is necessary to use these masks at an insecure non-domestic site.

5. Undetectable subversion that can be embedded in the complex designs of foreign-made components used in future defense systems.

6. Critical importance of electronics and its core silicon technology for providing a performance edge in a restructured DoD with a smaller but more effective force alignment.

7. Assured sources for DoD-unique microelectronics and electro-optics for NH&S (nuclear-hardened and survivable) systems.

These concerns and the pervasive importance of silicon technology to all defense systems were subjected to a Special Technology Area Review (STAR) and subsequently discussed for well over a year by Working Group B (Microelectronics) of DoD's Advisory Group on Electron Devices (AGED). The primary conclusion reached is that there is an urgent need for a new DoD investment strategy applicable to silicon technology—one that would be far more efficient and responsive to rapidly changing defense needs than the tactical approach now guiding technology development in this area.

III. DEFENSE RELEVANCE OF SILICON DEVICE TECHNOLOGY

In Desert Storm, data processing was provided in large measure by commercial personal computers. There were more commercial GPS position location receivers in the combat arena than those built to military specifications. This should not take away from the fact that the weapon systems were essentially electronic systems with weapons and their delivery systems attached. Silicon integrated circuit (IC) technology provided this core electronics capability.

Silicon IC technology for defense has been driven by system needs for higher performance and radiation hardness at ever-lower cost per function. Special-purpose silicon processors are pervasive across all military electronic systems. In radar, for example, they perform such critical functions as pulse compression, moving target indication, trajectory calculation, and tracking. In navigation they perform coordinate transformation, smoothing and prediction. In communications they are useful for spread spectrum receivers, adaptive channel equalization, encryption, adaptive antennas and bandwidth compression. In ECM and ELINT, they perform unique functions in search receivers such as adaptive filtering.

High speed parallel processing is key to advanced submarine detection and localization systems based on multi-array acoustic signal processing. It is also essential in multi-static radar systems that do not reveal their presence to precision emitter-locating systems, anti-radiation missiles or ECM receivers. In addition, silicion VLSI (Very Large Scale Integration) technology is extending the smart weapons concept to increasingly effordable fire-and-forget weaponry.

Silicon technology of VHSIC/VLSI complexity is capable of extending the performance of defense systems in a very fundamental sense—a dimensional sense. Whenever DoD extends its ability to see/protect/track/monitor a longer distance or resolve a smaller object/target, to build a larger or a smaller structure, to measure a shorter time or resolve a finer energy spectrum, it has advanced in a fundamental sense. These fundamental advances are made possible by increased signal processing and calculating capabilities found in advanced integrated circuits. Smart weapons embodying these advances are essential "force multipliers."

In the quest for new technological opportunities, DoD has been willing to accept high risks when warranted by the potential payoff in terms of real security. High on the list of those opportunites—and related technology issues—are these:

- Signal Processing Device Technology - Continued effort is needed to increase the density and performance of silicon processing devices through advanced packaging and device integration. Analog, digital and photonic device approaches are being explored to expand dynamic range, bandwidth, etc.

- Silicon-Based Multimaterial Devices - such as Si/Ge heterosturctures, GaAs and other III-V and II-VI compounds co-integrated on a silicon substrate, etc.

- Silicon-on-Insulator (SOI) Devices - for enhanced radiation hardness. Includes SOS (Silicon-on-sapphire), SIMOX (Separation by Implantation of Oxygen), Bonded, and ZMR/LSE (Zone Melt Recrystalization/Lateral Solid-phase Epitaxy) structures.

- Reliability/Test - to assure reliable component life throughout long life of military and NASA systems. New design tools, design-for-test strategies and quality assurance approaches—particularly QML (Qualified Manufacturers List) certification—promise to streamline this activity.

- Advanced Packaging/Interconnection Technology - the U.S. electronics industry is poised to make revolutionary advancements in the performance, size and weight, and cost reduction of electronic systems through adoption of greatly improved packaging, interconnect, cooling, and maintenance concepts at levels of integration beyond the chip level.

- Standards and Specifications - DoD should reexamine its specifications and standards to determine which reliability screens are still meaningful and which add cost but little value. Although a common set of silcon technology standards and specifications for both DoD and commercial industry would be desirable, reliability studies must continue to ensure that new materials and processes proposed for military-grade microciricuits will not cause problems at some future point, etc.

- Assured Sources - Parts obsolescance is becoming an increasingly serious problem. It has beeen estimated that the cost of redesign required to correct microcircuit nonavailability problems will exceed $2.9 billion in the next two to five years. The VHSIC Hardware Description Language (VHDL) offers a way to replicate in new technology the form, fit and function of earlier devices that may no longer be available.

- Rapid Prototyping - Two major efforts supported by DoD in the area of quick-turnaround manufacturing are the Microelectronics Manufacturing Science and Technology (MMST) program and Generalized Emulation of Microcircuits (GEM) program. Objectives call for development and implementation of flexible manufacturing methodologies that will permit rapid and affordable acquisition of advanced ICs for military systems by the mid-1990s.

A more detailed discussion of these high-payoff activities is given in Appendix D.

It is important to recognize that potential adversaries also understand the importance of advanced technology and rapidly acquire it when the opportunity arises. Although this was relatively difficult to do during the 1960s and 1970s, when the U.S. led the world in the defense application of IC technology, there is now state-of-the-art IC technology available from many global sources. This new state of affairs has had a twofold negative impact on national security: (1) in promoting the proliferation of high-tech weaponary, and (2) in having substantially increased DoD's dependency on foreign parts, materials and equipment.

Reversing these trends will not be easy. It will require a national policy that: (1) recognizes the importance of the U.S. silicon IC industry to national defense, and (2) is able to come to grips with the key reasons why the U.S. industry—and DoD—have fallen behind in certain key areas of silicon IC development and application. Chief among these reasons are:

- Loss, by U.S. industry, of its leading competitive position in high-volume semiconductor markets such as RAMs;

- Loss by the U.S. of leadership in some critical technologies such as semiconductor manufacturing and CCD image detectors; and

- U.S. industry difficulty in responding to DoD needs for small numbers of parts (usually requires long, costly development periods).

Regional conflicts are replacing global nuclear war as the more immediate threat to U.S. national security. The electronics technology for surveillance, communications, and simulation is becoming just as important as the technology that guides missiles to their targets. For these applications, the quality and reliability of commercial electronics is more than adequate. Clearly, in the next five to ten years a military taking advantage of the economy-of-scale benefits of superior commercial semiconductor production facilities will be best able to respond to any potential threat.

With the ending of the Cold War, the driving forces (rapid insertion of advanced technology, operation within a broader environmental regime, greater reliability and longer shelf life, and nuclear radiation resistance) behind DoD's quest for special defense electronic components have diminished. Commercial devices, with few exceptions, are at least equal in performance to military devices; they too are designed to survive harsh environments, to have higher quality and reliability and to require shorter development cycle time. DoD has much to gain from using commercial silicon devices.[6]

[6] Defense Science Board, Use of Commercial Components in Military Equipment, June 1989.

IV. TECHNOLOGY LIFE CYCLE IN DEFENSE SYSTEMS

Cutting-edge defense technology was heralded for inflicting a mortal blow to the command-control infrastructure and fighting spirit of Saddam Hussein's armed forces. It turns out, however, that the laser-guided smart bombs, TOW anti-tank missiles, Tomahawk cruise missile and Patriot anti-missile system cited as examples of that cutting-edge technology all use electronic components developed in the 1960s and 1970s. As a result, they all share the same problem: the components they use have been superseded by more advanced and lower cost product generations. The long lag between weapons development and deployment—often a decade or more—means components may no longer be available by the time spare parts are needed. Indeed, components designed into new weapons often become obsolete before those weapons even go into production.

Even more disquieting, Desert Storm highlighted the U.S. defense industrial base's growing dependence on foreign-made components. This problem was first identified in 1986 when the Defense Science Board found that unless an aggressive response was initiated, "advanced semiconductor technology simply would not be available within the United States to support the development of leading edge defense systems." [7]

Intensifying the spare-parts problem is the ever-shorter life cycle of new silicon IC products. In the case of DRAMs and SRAMs, for example, new product generations are now reaching the market every three years. The current 10- to 15-year lag between feasibility demonstration (6.2) and field introduction of military technology suggests that product obsolescence spanning four generations of memory technology could already exist. Somewhat longer intervals (five years for each generation) are applicable to other functions, such as microprocessors.

Two stopgap solutions are being investigated. The first is based on the "Generalized Emulation of Microcircuits" (GEM) approach, which is under the aegis of the Defense Logistics Agency. The second is the Microelectronics Technology Support Program (MTSP) under way at the Sacramento Air Logistics Center, McClellan AFB. It is both a technology replacement program and an effort to educate industry about alternative measures for dealing with parts obsolescence.

The VHSIC Hardware Description Language (VHDL) may be the long-term key to solving the parts obsolescence problem. Now an IEEE standard, VHDL has become widely accepted and will become even more important in the years ahead from both a device and system standpoint. For example, the top-down functional description of a system or component in VHDL enables low-cost exploration of system design options plus detailed understanding of system operation, while VHDL-driven design and process automation can provide for fabrication of replacement parts using current technology. In either case, however, designers must begin using VHDL today if its resultant benefits are to be ready in time to impact current systems.

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[7] Report of the Defense Science Board Task Force on Defense Semiconductor Dependency, February 1987.

The life cycle problem must be attacked on two fronts: system and technology. The first, encompassing system design, production, life cycle support, and the costs associated with these factors, is beyond the scope of this report. It is addressed elsewhere.[8] The second, technology, is amenable to increased use of software tools to manage the complexity of device and system interfaces, design, manufacturing, insertion, and procurement. It merits substantial investment, a recommendation that was strongly affirmed at AGED's recent STAR on Computer Aided Design. The principal recommendation that emerged from that STAR centered around the need for CAD tools to facilitate:

- Concurrent engineering of electronic systems
- Accurate modeling and concurrent simulation and optimization of performance, producibilty, cost, reliability, and testability
- Rapid, computer-automated translation of requirements to system, subsystem and microcircuit designs
- Automated system design upgrades in response to changing needs or technology obsolescence
- Technology-independent, computer-based functional descriptions

Clearly, VHDL will continue to be an important component of this software environment. However, additional tools are required to deal with analog/RF and mixed-signal designs as well as provide the capability to design, simulate, and produce the complex digital silicon devices of the future. Certainly, addressing these problem areas should be a high priority of DoD management.

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[8] Rapid Insertion of Electronic Technology (RIET) Workshop, November 1991, report in preparation.

V. STRATEGIC CONSIDERATIONS

The following are factors that must be considered in evolving a "Silicon Device Investment Strategy" for DoD that will guide it into the 21st century with a leading capability in defense electronics. Both the DoD and the industry technology environment are important.

DoD Factors Influencing DoD Silicon Investment Strategy

1. The resources available for investment by the DoD to ensure the military security of the U.S. will be limited. Maintaining a military force structure able to cope with continuing threats to world peace in the face of further downsizing of DoD programs, manpower and facilities in the 1990s will present a major management challenge.

2. There is a need to couple the defense industry more closely to commercial industry in order to maintain the technology and production capacity required for defense.

3. Military forces will become more dependent on high precision and highly effective weapon systems backed by intelligence and control, and less dependent on large numbers of men or platforms.

4. Strategic systems and nuclear warfare have become less pressing issues; rapid response and limited engagements have become more important. However, the proliferation of nuclear weapons and nuclear capability within third-world countries mandates continued development of effective IC-based countermeasures.

5. The trend is toward a unified military as the strategies and systems needed to cope with ground, air, sea, and space battles become less differentiated.

6. The trend will be to use standard system modules wherever common functional requirements exist—particularly since more of these modules will be implementable on single silicon chips.

7. Data and signal processing, control algorithms, and other electronic operations of complex systems will be implementable as small multichip modules attached to whatever input or output hardware is required. While high speed sensors and processors will use exotic semiconductors, processing of intermediate-speed signals will continue to be carried out by silicon-integrated-circuit-based parallel processors.

8. Co-design of hardware and software will be required for maximum operational integrity and flexibility in complex systems.

9. Production volumes of integrated circuits for specific military uses will continue to be small. Requirements for unique designs and for unique process technologies will persist but be limited to high value applications.

Industry Factors Influencing DoD Silicon Investment Strategy

1. The U.S. semiconductor industry in the year 2000 will have fewer than five broad-based silicon device manufacturers.

2. Industry and government are finding that their mutual interests are served best by increased precompetitive cooperation and coordination, particularly in generic R&D.

3. Restructuring caused by international competition has resulted in the virtual disappearance of long-range applied research in the U.S. electronics industry and it appears that this alarming trend will continue. Such long-range research provided much of the essential creativity that led to the success of the U.S. in the 20th century.

4. The pressure of global competition and rapidly growing markets will continue to keep commercial IC makers at the leading edge of technology. Even for ultrahigh speeds and broad environmental stress regimes, commercial devices will increasingly become the components of choice.

5. The infrastructure of the U.S. semiconductor industry has been decimated by competition. For example, silicon wafers, certain packaging materials, and some types of manufacturing tools now can only be obtained from foreign-owned suppliers.

6. Cooperative activities either through consortia such as the SRC and SEMATECH or through company-to-company agreements, both national and international, will characterize the industry structure of the future—driven by the need to share the high cost of development and production.

7. Need exists for high-volume fabrication facilities (fabs) and equipment as well as for flexible low-volume fabs.

Other Factors Affecting a DoD Silicon Investment Strategy

1. In semiconductors, it is impossible for the DoD to maintain a leading silicon device technology for defense use in a dedicated facility of any type that is independent of mainstream commercial activity. Defense electronics superiority is inextricably tied to global commercial integrated circuit superiority.

2. Cooperative activities represent the best way for DoD and industry to converge jointly on a common technology base for processing and design automation.

3. A hybrid system will emerge, encompassing DoD 6.1, 6.2, and 6.3a activities as well as industry product and process elements.

4. Standards, specifications, and procedures for both DoD and commercial applications must be merged, as appropriate, into a single set of standards covering all applications, except where no commercial equivalent exists—for high-dose-rate testing, for example.

VI. A SILICON INVESTMENT STRATEGY

A successful Silicon Investment Strategy requires objectives and an approach that are in consonance with the environment in which the strategy will be carried out. The associated implementation steps should be defined in broad terms and address an extended time period in order to provide flexibility in adjusting to results and changes in organizational environment.

DoD strategy must be closely coordinated with other cooperative industry and government efforts (SRC, SEMATECH, MICRO TECH 2000, etc.) focusing on silicon devices and technology—both to avoid redundant efforts and to leverage the investments made by these other activities. In fact, the need for a DoD strategy is actually increased by the very existence of these other technology efforts—to ensure that adequate attention is paid to defense priorities. In turn, DoD must support these other technology efforts—again to ensure that its needs will be served.

OBJECTIVES - The main objectives of a DoD Silicon Investment Strategy are:

1. To address the concerns of DoD by:

   a. Ensuring continued access to leading-edge silicon integrated circuit technology for defense system applications.

   b. Ensuring sources for defense-critical integrated circuits for the life of systems.

   c. Providing for security in the fabrication of highly sensitive integrated circuits.

   d. Ensuring integrated circuit sources that do not pose a subversion threat.

   e. Meeting the electronics-based warfighting needs of this nation's future force structure, however altered.

   f. Ensuring, in particular, that rad-hard, space-qualified and other military-unique devices are available from multiple sources.

2. To leverage, to the fullest extent possible, advances in commercial integrated circuit technology and to catalyze, when possible, other technology investments in meeting defense needs.

3. To ensure that the best technology is available within the U.S. in the most critical areas.

4. To provide continuing capability projections to guide both the Silicon Investment Strategy and defense system planning and development in general.

5. To respond rapidly and affordably to unique technology needs of defense systems.

6. To provide for the most effective use of organizational, budgetary, and manpower resources.

7. To provide a basis for establishing priorities for DoD investment in silicon technology.

APPROACH - The following policy considerations and recommendations form the basis of the desired DoD Silicon Device Investment Strategy:

1. It is not productive for DoD to create or operate additional fabrication or production facilities or lines to produce silicon devices solely for defense applications. Emphasis must be on exploitation of commercial production lines. The lone exception should be a single facility, operated in a close relationship to commercial production, that would serve as a source of devices requiring the highest level of security—for example, cryptographic and command encoders.

   As part of this policy, resources now used to support captive or military production lines, including system and IR&D funds, would be diverted to more productive areas, such as those defined below. In addition, defense-unique designs, such as EW signal processors, would be fabricated almost exclusively by commercial production lines. It should be recognized, however, that for this to happen, some enabling legislation will probably be necessary.

2. R&D funds should be directed to advance the state of the art of the combined U.S. military/industrial semiconductor industry, with emphasis on those areas that respond best to defense needs. For example, nonvolatile memories (NVMs), static random access memories (SRAMs) and microprocessors that are key to defense applications should be strongly supported. Because of the dependence of these devices on mainstream silicon technology, one of the primary objectives of DoD investment in this area should be the achievement of a robust commercial product capability that also serves defense needs.

3. Particular emphasis should be placed on the development of comprehensive and computationally efficient models and simulation tools capable of dealing with the multitude of process steps involved in modern microchip design/fabrication—and to facilitate the advance to deep submicron (< 0.35 micrometer) devices.

4. Design automation and its extensions into the total software environment concept for defining, designing, and producing state-of-the-art silicon chips should be advanced through appropriate resource investments, as was recommended by the CAD STAR (see p.11).

5. DoD should support R&D that is at the forefront of technology but whose high risk discourages industry investment. This applies to such technologies as X-ray lithography and the conception and demonstration of totally new device concepts—devices that may prove to be of critical importance to U.S. military systems of the 21st century.

6. DoD should continue to support development of technologies needed to satisfy unique requirements, such as rad-hard and space-qualified devices.

DOD SILICON INVESTMENT STRATEGY

APPENDICES

Appendix A

SILICON DEVICE TECHNOLOGY CHAIN

The semiconductor technology chain includes those activities and resource applications that extend from research aimed at the creation of new understanding through the development and fabrication of components for fieldable defense products, from computers to missile systems. The technology chain involves a large number of organizations and technology agendas. Links of the chain are described in various ways but most generally are defined by the structure of the technology base. Within DoD, the 6.1, 6.2, ... sequence is employed to structure the technology agenda.

No aspect of the technology chain concept is more important than the necessity to balance investments and resources in each link of the chain to obtain optimum benefits. Defense efforts often have tended to neglect one link in the chain, thereby negating the benefits obtained from investments in other links.

Activities along the DoD semiconductor technology chain become increasingly application specific as one moves toward the final product. The first link in the technology chain, its root, is basic or fundamental research. The final link is a new semiconductor device or module earmarked for some DoD application. Between the ends of the chain, parallel branches exist that ultimately converge to form links in the primary chain. Manufacturing methods, component and system design, and the core device and processing technologies constitute major branches, each creating a core capability essential to new semiconductor products.

Ultimate applications of new silicon devices are in systems. Although the system technology R&D chain is beyond the scope of this discussion, some of its aspects provide significant challenges for the device community:

- First, there is the challenge of persuading systems development organizations to accept and apply new device technology. They are understandably quite cautious; thus the credibility of the new technology must be very high and the risk low.

- Second, there is the challenge of finding a way to shorten the time between the creation of a new component technology and its appearance in a fielded system. At present, the technology is often commercially obsolete before it first appears in a DoD application.

- Third, there is the challenge of supporting system device needs long after the commercial life cycle of the device is completed and production has ceased.

Additional challenges and problems abound, stemming form procedures and paperwork that inflate device costs by 10 times or more, qualification requirements that increase costs but not reliability, the tendency on the part of DoD to try to create—often on a wasteful crash basis—

unique devices for each system, and DoD's predilection for investing in R&D efforts that result in never-produced, sometimes unproducible, devices. The DoD device community must find ways to meet these challenges if it wishes its role to continue to grow.

The major lessons to be learned from the holistic view is that there are persistent weak links in this chain that often prevent the DoD from reaping the benefits of superb laboratory efforts. Efforts such as VHSIC or SEMATECH, designed to strengthen recognized weak links, are not successful unless the strength of the other links of the technology chain are maintained. With funding limitations, it is often difficult to strengthen a weak link without weakening other links in the process.

The following describes the structure of the semiconductor technology chain and lists the significant components of each link. This description is neither unique nor necessarily complete for all of the various purposes to which it might be applied.

BASIC RESEARCH

Exploratory research to gain a better understanding of phenomena and materials without specific concern for applications.

Physics	Chemistry	Materials	Computer Science

FOCUSED/APPLIED RESEARCH

Research to increase knowledge, preferably through models, in specific fields that are associated with identified applications or needs.

Materials	Devices	Techniques	Phenomena
Reactions	Metrology	Properties	Lithography
Interconnections	Processes	Packaging	Design tools

ADVANCED DEVELOPMENT

Efforts to demonstrate applicability of research, to define the parameters of new knowledge resulting from research, or to search for generic results applicable to classes of problems or needs.

Integrated circuits	Analysis	Insulating layers
Bipolar technology	Testing	Manufacturing processes
CMOS/BiCMOS technology	CAD	Interconnections/contacts
Silicon wafers	CIM	Analytical tools

PRODUCT DEVELOPMENT

Efforts to demonstrate products or techniques that meet predefined parameters and/or satisfy specific needs.

Integrated mfg. system	1 Gbit SRAM	A/D converter
Microprocessor	Signal processor	Ion implanter
Plasma etcher	12 inch wafers	Testers

PILOT PRODUCTION

The application of combined manufacturing, device, processing, and quality-assurance tecniques to the actual production of devices or components for defense applications.

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There are breaks in the chain when technology research and development efforts are carried out by different organizations—for example, 6.1 - universities, 6.2 and 6.3a - Service laboratories and industry; IR&D - prime contractors and suppliers; specific parts development - prime contractors; and actual production - primes and suppliers. The integration and application of technology emerging from DoD laboratories, prime contractors, and suppliers is an important challenge that is not addressed well within the existing framework.

Appendix B

KEY SILICON DEVICE TECHNOLOGIES

DEFENSE SILICON TECHNOLOGY

Design, fabrication, and application of silicon integrated devices requires a wider variety of techniques and tools than almost any other manufactured product. Hundreds of steps are required to fabricate the multimillion-transistor chips now being incorporated in electronic systems. Some of these steps require the best optics known to man, the purest materials that exist, the highest precision control, the most complex tools, the cleanest factories, and the most powerful design aids.

The challenge for the integrated circuit R&D community is to advance simultaneously in all of these areas at the rapid pace required to maintain the frenetic advances of the last three decades. For defense technology, if the best integrated circuits are to be available and defense concerns met, a demanding development pace will be required to at least maintain parity with—and preferably surpass—the capabilities being developed in other countries, especially since foreign devices may be made available to the military systems of potential adversaries.

To provide a technology perspective for a DoD Silicon Investment Strategy, a brief overview of some of the key silicon device technologies is presented below:

ACTIVE DEVICES

The core structure in any silicon integrated circuit is the active transistor. Today's dominant transistor type, the "MOSFET," is being designed in increasingly sophisticated form as design rules shrink. This downscaling trend, which has led to faster and more complex chips, will continue for the foreseeable future, though at a gradually slowing pace. (Initially, simple dimensional scaling allowed tighter design rules and thinner gate oxides and, consequently, the creation of smaller transistors with higher speed and lower power. Now, changes in the device structure itself are becoming necessary to cope with the effects of ever-smaller geometries.)

From a technology investment point of view, it now appears that:

- The commercial sector will continue to develop higher-performance, low-cost silicon technologies for microprocessors, DRAMs, SRAMs, ASICs (application-specific integrated circuits) and analog circuits for at least the next decade.

- Compound semiconductor technologies will provide ultrafast circuitry for both analog and digital circuit functions, but only in relatively simple chips and at a significant cost penalty per function compared to silicon.

- DoD's need for an ultrafast technology offering a high level of integration is essentially limited to complex signal processing. It turns out, however, that such technology is more advanced than the more cost-effective, high-volume state-of-the-art technologies of the commercial sector. For such applications, the e-beam lithography eschewed by industry as inappropriate for high-volume production would appear to offer a suitable way to service the small-volume needs of DoD.

COMPUTER-AIDED DESIGN (CAD)

CAD is the process of converting a product description, performance requirements, and business constraints into a design, manufacturing, and test specification. It requires the development of specifications at all intermediate levels of design, including behavior, register-transfer, logic, circuit, routing, layout, device, and fabrication process, and encompasses simulation, optimization, and testing. As indicated below, accurate modeling of all these steps will continue to be critically important. Libraries of macrocell designs are employed in the compilation of system functions on a chip. Macrocells implement standard functions such as adders, correlators, switches, and cache memory. Although proprietary CAD capabilities have been developed by major semiconductor manufacturers, most CAD needs are now served by commercial vendors of computer programs, many of which are adaptations of university-developed software and concepts.

Major CAD challenges include gaining the ability needed to design the increasingly complex chips of the next decade, reducing the high costs associated with the design of today's chips, and integrating design, fabrication, testing and application software into a single unified system.

LITHOGRAPHY

Lithography, the conversion of designs to masks and the replication of those masks onto silicon wafers, remains the pacesetting fabrication technology. It is continually challenged to provide capabilities for rapid throughput of wafers with finer geometries while avoiding the killing defects that limit process yields. Although 1:1 lithographic tools are still used, the tool of choice is now the optical reduction stepper in which the mask pattern is reduced in size and repetitively projected onto the photosensitive resist, coating the wafer until the entire wafer has been imprinted with the desired pattern. An adaptation of the optical scanning technology used for previous generations of lithography is also being introduced. It combines reduction, scanning, and stepping to obtain full wafer coverage and uses reflective optics. Metrology needs are pervasive.

Current major challenges associated with lithography include incorporation of phase shifting masks in the process to obtain greater resolution with the available optics, developing optics for 193 nanometer optical wavelengths, solving the control problems (including metrology) at 0.1 micrometer dimensions, ascertaining the capabilities of X-ray lithography as an economic solution for 0.35 micrometer and smaller dimensions, and the design of reliable, high-throughput tools that incorporate the best technologies.

WAFER PROCESSING

Wafer processing involves the deposition and removal of various materials (metals, insulators, and semiconductors) in conformity with the highly precise lithographic pattern, and the cleaning of the coated wafer. Modern techniques require control of deposition and removal of materials in layers down to 10 atoms thick and with laterally defined dimensions as small as 0.1 micrometer. New forms of selective deposition and removal are being vigorously pursued. Technologies include chemical vapor deposition, laser-induced deposition, evaporation, sputtering, ion implantation, plasma and wet etching, and rapid thermal annealing.

The major challenges in wafer processing include: obtaining sufficient understanding of processes so that they can be modeled for optimization and precision control, developing advanced fabrication tools capable of affordably implementing all processes on a high-yield/high-throughput basis in a production environment, and extending the performance of the tools to the deep-submicrometer geometries required in the next decade. New low-temperature process capabilities will have to be established to meet the low thermal budgets required for the fabrication of giga-transistor chips.

MODELING AND SIMULATION

Modeling and simulation are essential not only for device design and processing, but for materials, systems, reliability, and factory operations as well, driven by the need to manage and control the complex knowledge required to design, develop and fabricate high-tech products and minimize costly experimentation. While circuit, device and process models have been developed for over two decades and have contributed significantly to the advancement of device technology, the pace of new materials and technology advances has been so rapid that development of new device and process models and computationally efficient simulation capabilities has had great difficulty keeping up.

Complexity issues have led to the definition of a regime of CAD called "technology CAD," or TCAD, where modeling is focused on circuits, devices, and processes—in contrast to subsystem and system CAD, which is drawing a growing amount of design automation and computer integrated manufacturing (CIM) interest.

Challenges in simulation include evolving a TCAD framework and then extending the models to 3-D structures. Within this framework, a set of physically and empirically based models is required for devices and processes, extending to the atomic scale. Visualization must be incorporated in the models to provide user-compatible input/output capabilities. The metrology for getting data to use in developing models, measuring the performance of tools and processes, and controlling variables (temperature, gas flow rates, etc.) in the tools and processes does not now exist. Models must be extended vertically to the system level and horizontally to a multiplicity of designs and processes.

MATERIALS

The U.S. position in silicon and compound semiconductor materials production as well as in other areas of electronic materials is weakening. For many years the focus of IC-related materials R&D has been the attainment of higher quality and larger silicon wafers, better quality and lower temperature deposited insulators, and improved conductor systems for contacts and interconnections. While that work continues, more exotic material systems are now being considered to satisfy the needs of submicrometer-geometry device structures and the desire for additional functionality. Ferroelectric, ferromagnetic, conductor, insulator, and semiconductor material systems are being improved and their applications demonstrated. The heteroepitaxial demonstration of GaAs, Ge_xSi_{1-x} and $Ge_xC_ySi_{1-x-y}$ for IC bandgap engineering, the use of $BaTiO_3$ and $Pb(Zr,Ti)O_3$(PZT) for nonvolatile DRAMs, and the use of copper as a low-cost alternative to the aluminum conductors on ICs are examples.[1]

Among the advanced materials needed for submicrometer devices are dielectrics with both higher and lower dielectric constants, insulators with higher thermal conductivities, fine-line conductors capable of cost-effective downsizing and reliable interconnection, and semiconductors capable of both efficient photon emission as well as compatibility with silicon substrates.

MANUFACTURING

Silicon integrated circuit manufacturing is one of the most complex processes undertaken by industry. Hundreds of process steps are entailed in moving from the purchased silicon wafer to the packaged integrated circuit ready for sale. Despite the importance of these process steps to the quality of the ICs themselves, most of the key manufacturing equipment required to process these devices is now made by non-U.S. companies. This is recognized as a major weakness of the U.S. industry and has been the focus of the SEMATECH effort. In addition to effort aimed at strengthening U.S. semiconductor equipment capabilities, process models and computationally efficient simulation capabilities, procedures and software are being improved as part of a concerted effort to eliminate this weakness.

The major challenge is to evolve an integrated circuit manufacturing line capable of producing small lots of many different designs with first-run success. A second major challenge is the attainment of a much higher degree of predictability and control, and thus higher yields, in factories producing large volumes of only a few designs. In both cases, the approach being taken is to use proven U.S. skills in systems and simulation to create a factory software environment that provides the required control and flexibility.

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[1] AGED STAR report on Silicon-Based Multimaterials Technology, November 1990.

PACKAGING AND INTERCONNECTION

Integrated circuit packaging is viewed by many as the Achilles' heel of the U.S. technology base, having been virtually forfeited to foreign practitioners and suppliers. Even the most critical of integrated circuits are often assembled into packages composed of piece parts made by foreign suppliers at an offshore location. However, prospects appear to be brightening again for the U.S. in this area as a result of several recent advances. One of the most promising of these advances involves the multichip module (MCM) concept which depends on the ability to package many chips on a common substrate with a very large number of high-performance interconnections.

Aside from solving the technical problems associated with MCMs and implementing MCM technology in U.S. factories, the biggest challenge will lie in the area of chip testing—that is, testing the chips prior to their insertion into the MCM. Another challenge will be the development of design tools for integrated circuit packaging that will result in system architecture optimization as well as allow prediction of electrical and thermal requirements with greater accuracy than now possible.

TESTING AND "BIST"

Testing gigascale chips is difficult. Publicized instances in which design errors have been found only after a chip has been used in large numbers of applications illustrate the difficulty of complete testing. Interactive faults within an integrated circuit may escape detection and appear only when called upon in a critical operational application simply because the number of system states exceeds the coverage afforded by existing simulation and test generation approaches. One approach used to ease this problem calls for dedicating part of the chip design to internal test capabilities. This is referred to as built-in self-test (BIST) and is an expensive solution. Major challenges confronting the test community include the refinement and application of BIST, the development of more efficient and higher performance testing systems, and the realization of test strategies that will provide the assurance levels required for critical system applications.

CLEAN ROOMS, CONTAMINATION, AND YIELD

Fabrication facilities are closely associated with manufacturing technologies. Defect-free wafers require contamination-free processing environments characterized by clean wafer transport systems, gas and process chemical purification techniques, sensitive detectors, hands-off equipment and lights-out factories, and other pristine measures and close process control needed to produce future devices.

Further yield enhancement in future semiconductor fabrication will similarly require development of increasingly stringent clean-room and other contamination-control procedures and strategies. Reducing the physical size of the wafer environment so that it is never exposed to the factory air, more fully controlling the processing environment in general and various pieces of process equipment in particular, and completely automating the process so that wafers need never be exposed to operators are among the techniques being investigated.

RELIABILITY

There is no surefire method for demonstrating the reliability of a modern integrated circuit. To determine the reliability required of ICs used in systems that may sit on a shelf for years and be required to operate without fault in a stressed environment demands approaches different from any used in the past. More attention will have to be paid to designed-in reliability, fabricated-in reliability, physics of failure, and microscopic defects. Killer defects will be as small as 0.01 micrometer. Measuring the size and concentration of particles that small is beyond the present state of the art.

The challenge is to develop the concepts and approaches to system reliability assurance that will meet future requirements.

MAJOR TRENDS OVER THE NEXT DECADE

Within the next decade, silicon integrated circuits will become available with over a billion transistors residing on a chip less than 1 square inch in area and with logic speeds of 500 MHz or higher. Since most current system functions will be implementable on a single chip of this complexity and memory capabilities will expand by orders of magnitude, the capabilities of defense systems will expand greatly. Intelligent fire-and-forget missiles with the ability to recognize specific targets will be possible; completely new warfare scenarios will be developed to take advantage of these new technology-based system capabilities; the reduced weight of electronic systems will enable smaller and better weapon platforms; and near-instantaneous information processing and response times will be possible.

It is imperative that these capabilities become available to U.S. forces before they become available to those of other nations. A technology-based force-multiplier strategy with a silicon investment strategy as one of its key elements is clearly the best way—if not the only way—to ensure that this will be the case in the year 2000 and beyond.

Appendix C

U.S. SEMICONDUCTOR TECHNOLOGY BASE

The U.S. semiconductor technology community has many contributing participants, ranging from vertically integrated corporations that are active at every level in the technology chain (research, chip production, subassemblies, and electronic system applications) to single-function organizations with very focused roles (design, tool manufacture, packaging, research). In addition to industry participants, there are government, university and other organizations (such as cooperative groups and research institutes) active in this area. This diversity is a strength that should be protected even as productivity-enhancing measures are considered and implemented.

Although there are many linkages between these different activities, both through the interaction of individuals and organizational ties, it would be misleading to say that the research activities are particularly well integrated or even coordinated.

The U.S. semiconductor technology base is unmatched in its latent capabilities. If properly utilized, it could readily provide the knowledge and tools needed for succcess. The U.S. does not need to increase the number of research organizations; it must, however, strengthen them and use them more effectively.

The structure of the technology base is shown in Table C-1. All types of organizations perform R&D to a greater or lesser extent. The largest R&D effort, by far, is found within the semiconductor device manufacturing industry, which spends about 15 percent of its gross revenues on R&D. This comprises about 80% of the total U.S. expenditure for semiconductor device research, which, for both merchant and captive producers, is estimated to be more than $4 billion annually. However, competitive pressures on this industry segment have forced an increasingly short-term focus onto that investment, with the result that longer-range strategies and research objectives are no longer being adequately addressed.

Over the last decade, the U.S. semiconductor industry has come to realize that cooperative R&D has much to offer. Vigorous international competition, with significant cultural and business environment advantages available to foreign industry, has caused the U.S. semiconductor industry to lose over one percent of market share each year for over 25 years. To truncate or reverse this trend will require significant changes in the procedures, practices and environment of the U.S. industry. One such change is to make better use of R&D investments through cooperation.

Industry actions stemming from the realization that cooperation in technology is a necessary step have resulted in the creation of the Semiconductor Research Corporation (SRC) and, more recently, SEMATECH.

TABLE C-1
U.S. SEMICONDUCTOR TECHNOLOGY BASE PARTICIPANTS

Industry
- Semiconductor device manufacturers
- Tool and test equipment manufacturers
- Materials and software suppliers
- IC design houses
- Semiconductor device users
- User industries - computer, aerospace, defense, etc.

Government
- DOE - national laboratories/research program
- National Science Foundation
- National Institute of Standards and Technology
- DoD - DARPA, Service laboratories & research offices
- GoCo laboratories

Other
- Industry cooperatives - SRC, SEMATECH, MCC
- Universities
- Not-for-profit research institutes
- State research organizations

The SRC was created in 1982 to address long-range generic research and skilled manpower needs cooperatively. It has been a highly successful cooperative, funded primarily by the semiconductor industry, but with government participation as well. The SRC has provided a consensus semiconductor research strategy and road maps for its implementation. SRC support of university research has successfully restored and preserved vital semiconductor research activities in universities and has initiated academic study of a number of increasingly important associated semiconductor topics, such as packaging, reliability, and manufacturing.

SEMATECH was founded in 1988 to address cooperatively the very critical need for upgrading the semiconductor industry's manufacturing capabilities, particularly its fabrication tools. It is a joint technology development effort of the DoD and U.S. semiconductor industry to provide the critical capabilities for manufacturing successive generations of semiconductor products. It

conducts a strong in-house development and demonstration activity and works closely with U.S. manufacturers of semiconductor fabrication equipment to provide state-of-the-art tools for semiconductor manufacturers.

In 1991, the industry and government together, acting through the National Advisory Committee on Semiconductors, defined a broad initiative called MICRO TECH 2000 that is directed toward increased integration of the disaggregated technology base through cooperative efforts to address a defined set of technology goals. These goals are benchmarked in terms of a gigabit SRAM which, if achieved by the target date proposed, the year 2000, would provide the U.S. industry with world-leading semiconductor technology capabilities by leapfrogging, by one device generation, the state of the art that would otherwise exist at that time.

There are a number of other "cooperative" organizations that participate in some way in semiconductor R&D, although they do not necessarily exist for that purpose. These include industry organizations like MCC, state organizations like MCNC and MMC, university-organized industrial liaison programs, and government-funded research centers.

The research agenda with which these organizations are concerned is diverse and requires the participation of both scientists and engineers from a variety of disciplines. It is unlikely that any one organization could address all of these areas, or, even if it could, muster the resources necessary to do an adequate job.

At present, the competition within the industry and the diversity of the technology base has prevented much meaningful coordination of this technology agenda. The general rule is that each organization—often each researcher—sets its own goals. The result is that a large part of the U.S. R&D investment is dissipated through redundancy and repetition. The challenge, recognized by MICRO TECH 2000, is to somehow bring a higher degree of order among the large number of diverse organizations now participating in semiconductor R&D without conflicting with their organizational goals or inhibiting their creative and innovative abilities. The biggest challenge is to find additional opportunities for cooperation among the most significant semiconductor R&D segment, the semiconductor manufacturing industry. In this regard, SEMATECH has made enormous progress in establishing cooperative activities in the technology areas associated with manufacturing, the area of greatest need and largest potential impact. Much more remains to be done, however.

In addition to the approximately $4 billion invested annually by the semiconductor manufacturing industry in R&D, an additional $0.5 billion each is invested annually by the suppliers to that industry (equipment, materials, etc.) and by the U.S. government, for a total of about $5 billion. Integration/coordination of the activities of these participants is highly important as well.

Although relatively small and largely focused on defense-related needs, the government effort nevertheless is capable of providing large benefits to the technology base, particularly in longer-range generic research areas, and of providing important resource sharing, other incentives, and leadership in cooperative activities.

It is conceivable that, through increased cooperative activities, the effectiveness of the nation's investment in semiconductors could be increased by more than 20%, which would be equivalent to adding $1 billion a year to the advancement of semiconductor technology development in the U.S.

Cooperation can consist of many forms: vertical cooperation between suppliers, manufacturers, and users of semiconductor devices; horizontal cooperation in generic technologies among competitors; and industry cooperatives in which competitors combine resources in organizations that address common purposes. Sometimes variations of these cooperative forms develop. For example, SEMATECH, although primarily a horizontal form of cooperation among semiconductor manufacturers, includes equipment and material suppliers in joint efforts. This has motivated the creation of SEMI/SEMATECH, which is a horizontal cooperative organization of suppliers to the industry.

Appendix D

SPECIAL NEEDS OF DEFENSE

The major elements of U.S. defense policy—strategic deterrence and defense, forward presence, crisis response, and force reconstruction—have not changed with the dismantling of the USSR. Strategic and tactical military systems, making use of increasingly sophisticated electronic components, will still be needed to cope with a broad spectrum of future threat scenarios. As in the past, silicon technology will continue to be at the core of most of those components and systems for the foreseeable future.

Silicon IC technology has led to system-performance breakthroughs in space, under and on the sea, and on the land battlefield. The common denominator in these diverse tactical and strategic applications is the computational power provided by the U.S. silicon IC industry and its manufacturing base. In the last decade alone, complexity times speed has increased by three orders of magnitude while computing costs have decreased by at least three orders of magnitude. Further gains and innovations in silicon technology will have dramatic effects on national security. In the next 10 to 15 years we can expect to see:

1. Integrated intelligence, target acquisition and weapon delivery systems—a combination that some have dubbed "the ultimate force multiplier."

2. A new generation of ASW systems that not only detect but also localize quiet submarines for targeting.

3. Air defense systems that are extremely resistant to detection, jamming or destruction.

4. Really smart weapons that pursue and attack specific targets.

5. Autonomously guided precision conventional weapons such as cruise missiles. (Because of their accuracy and effectiveness, such weapons lessen the need for nuclear weapons.)

6. Improved equipment maintenance and reliability derived from neural networks and other new computer techniques instead of from complex sensors and skilled manpower.

7. A new generation of autonomous, long-lived satellites for surveillance.

DoD's special tactical and strategic needs are summarized in Table D-1. Figure D-1 shows that these needs are tied inextricably to broad areas of silicon IC/VLSI technology. It is because of the pervasiveness and importance of silicon technology to these needs that an investment strategy dedicated to the advancement of silicon technology is so necessary.

TABLE D-1
DoD SPECIAL NEEDS

TACTICAL

Naval Warfare

- Ocean Surveillance & Anti-Surface Ships
- Undersea Surveillance & ASW
- Mine Warfare & Countermeasures

Air Warfare

- Close Air Support & Battlefield Interdiction
- Interdiction/Naval Strike
- Defense Suppression
- Counter Air

Land Warfare

- Close Combat
- Ground Air Defense
- RECCE, Surveillance & Target Acquisition

Theater and Tactical C^3I

- Command and Control
- Tactical Information/ Intelligence Systems
- EW & C^3 CM

Defense-Wide C^3I

- Position and Navigation
- National Intelligence
- Intelligence to Tactical Forces

STRATEGIC

Strategic Defense

- Warning
- Air Defense
- Ballistic Missile Defense
- Defense suppression
- Space Defense Initiative

Strategic C^3I

- Command and Control
- Communication

As for the future, the projected growth in military system functional and performance requirements will continue to place ever-greater demands on semiconductor technology—particularly in terms of life cycle cost, power consumption, weight, volume and reliability. Unless these challenges are met by means of an effective investment strategy, many critical and innovative weapons systems concepts will remain on the drawing boards or stagnate in the development phase because of the inability of the technology base to provide the capabilities necessary to meet known and projected threats which could become the national security issues of the mid- to late 1990s and early 2000s.

DEPARMENT OF DEFENSE NEEDS			SILICON STRATEGY		
			IR FPA • Materials • Devices • Arrays • FPA SP	COMPUTING VLSI • Processors • Parallel SPs • Software	SYSTEM VLSI • ATR • ANNs • C^3
STRATEGIC	STRATEGIC C^3I		•	•	•
	STRATEGIC DEFENSE		•	•	•
TACTICAL	DEFENSE-WIDE C^3I	Position & Navigation	•	•	•
		National Intelligence		•	
		Intelligence to Tactical Forces	•	•	•
	THEATER & TACTICAL C^3I	C^3		•	•
		Tactical Information/Intelligence Systems	•	•	
		EW & C^3 CM	•	•	•
	LAND WARFARE	Close Combat	•	•	
		Ground Air Defense	•	•	
		RECCE, Surveillance & Target Acquisition	•	•	•
	AIR WARFARE	Close Air Support & Battlefield Interdiction	•	•	
		Interdiction/Naval Strike		•	
		Defense Suppression	•	•	•
		Counter Air	•	•	•
	NAVAL WARFARE	Ocean Surveillance & Antisurface Ships	•	•	•
		Undersea Surveillance & ASW	•	•	•
		Mine Warfare & CM		•	•

FIGURE D-1. SILICON STRATEGY RELATED TO DoD NEEDS

Among the key technology requirements expected to remain important in this area are ultrahigh reliability and fault tolerance, increased functional throughput, and improved radiation hardness—all implemented in the context of the highest product quality and based to the fullest extent possible on mainstream commercial product capabilities. The solution to the common denominator found in many warfare areas—as varied as space-based electronics, antisubmarine warfare, "really" smart weapons and command and control—is in highly integrated, totally compatible silicon VLSI disciplines. If DoD is to meet these requirements and gain access to products that are technically superior and affordable, it will have to rely far more on commercial technology.

These application needs translate to needs in basic capabilities and quality in all disciplines of silicon VLSI manufacturing technology. Without this capability, smart weapons, for example, would fail to perform effectively the many sensor, information processing, and control functions that are required. To handle 10^{12}-10^{15} FLOPS, processors will require the technological capability of 10 to 100 million transistors integrated in a single VLSI chip, each chip delivering 250 to 1,000 MFLOPS, the equivalent in computational power of two to 10 CRAY-1 supercomputers. Silicon technology offers the promise of satisfying these required information fusion and processing capabilities. For example:

- Full-ocean-basin surveillance, based on the coherent multi-array processing of a few thousand beam intersections with narrow frequency bins, requires between 100 and 1000 GFLOPS in computational capability.

- Synthetic aperture radar (SAR) processors for aircraft applications should provide 700 MFLOPS to allow a combination of increased field of view (1200 x 1200 pixels), 5 foot resolution, and automatic target location in unconstrained flight conditions.

- Affordable, monolithic silicon infrared CCD focal plane arrays, based on Pt-Si or Ir-Si detectors, with $\geq$ 1024 x 1024 pixels (detectors) and on-chip processing, have implications for imaging and non-imaging, strategic (space surveillance and target acquisition) systems; for sensors for aircraft, ships, and battlefield remotely piloted vehicles; and for tactical IR missile launch detectors, passive artillery and mortar locators, and fire-and-forget missiles.

- Electronic intelligence (ELINT) involves very low power (< 1 mW) signal analysis, wideband data communications and wideband spectral analysis, but is severely constrained by current system performance, which cannot meet the required throughput of 500 MFLOPS. Concomitant with the requirements for these processor throughput rates, large memories are also needed. A space-based SAR radar with 200-500 MFLOPS of computational power needs 4 x 10^7 bytes of memory. Similarly, the estimated memory requirement for an airborne ASW signal processor providing passive surveillance, IFF, radar surveillance, missile targeting, periscope detection in clutter, sonobouys and navigation processing is in excess of 8 x 10^9 bits or 2.5 x 10^8 32-bit words.

TECHNOLOGIES FOR DEFENSE

Signal Processing - Signal processing provides the bridge between raw data and useful information. It is no wonder, therefore, that signal processing technology—primarily in the form of silicon IC/VLSI technology—has been fundamental to meeting DoD objectives in surveillance, communications, command and control, electronic warfare, avionics, and intelligence. Clearly, it will continue to play a key role in meeting increasingly difficult challenges relating to surveillance and classification of small targets in a severe clutter/jamming environment, jam-resistant covert multiband communications, multimode control of fighter aircraft, and advanced-intelligence workstations.

Signal processing technology is pushed by major advances in underlying circuit technologies and pulled by the needs of military, commercial, industrial and other users, each steering the technology to a lesser or greater extent. It is up to DoD to ensure that its needs—for high throughput, high reliability, maximum security, and adequate radiation hardening, as well as for strict power, weight, and volume limitations—are effectively addressed. Silicon device technology has provided and will continue to provide the primary building blocks for meeting DoD's needs. Because currently defined defense requirements for signal processing capabilities exceed those of the other users, it is appropriate that DoD assume leadership in this area with an effective Silicon Investment Strategy.

To achieve higher density and better system performance, effort is being increasingly focused on the exploitatation of advanced packaging and on the use of special-purpose, highly integrated devices. Analog and digital electronic devices as well as photonic devices are being pursued in the quest for increased dynamic range and bandwidth.

Merged and Multimaterial Technologies - Gallium arsenide devices run at multi-gigahertz speed while silicon devices are generally limited to megahertz rates. GaAs devices run off low voltage supplies and can provide microwave functions while silicon devices are considerably more dense, consume much less power, and are far less expensive to manufacture. Clearly, a monolithic technology capable of integrating the most desirable features of GaAs and silicon devices would be beneficial because:

- No single device technology can meet all subsystem circuit requirements;
- Integration would reduce power dissipation and increase speed by reducing parasitics and transmission line I/O delays;
- It could lead to high speed GaAs processors co-integrated with dense, low power memory;
- GaAs-on-silicon is a potential future replacement for BiCMOS when voltages drop to 3.3 volts and lower; and
- GaAs-on-silicon integration provides a more direct path to an optical interface.

To take advantage of the inherent characteristics of each technology, co-integration on a common silicon substrate is deemed a desirable solution to very-high-performance, low-power integrated circuit technology capable of operating in military environments. Although problems cited at the "Multimaterial STAR"[2] remain, results on materials growth and low-temperature processing indicate that electronic-device-quality material can become a reality.

Recent progress in silicon/germanium materials and device technology has been very encouraging and should be a key part of an overall multimaterial program. Both bipolar and FET devices should be included.

While a major new initiative is not warranted at this time, many fundamental problems remain and should be addressed at the present or slightly increased level of effort.

Radiation Resistance - SOI - In the general area of radiation-tolerant silicon devices, there is only a limited non-governmental marketplace. Commercial satellite systems and commercial nuclear power control are the only non-defense/non-governmental users of high-reliability, radiation-tolerant silicon devices. All other users and developers are developing systems either directly or indirectly for defense or government applications. Export of these types of devices is controlled under MCTL 2.0, 7.1, and ECCN 1564A, 1565A, and 1574 because of national defense and nuclear proliferation risks. Marconi is the only known competitive foreign source.

Silicon-on-insulator (SOI) technology has long been of interest to DoD because of its superior radiation-hardness characteristics (relative to bulk silicon). Besides improved radiation resistance, it offers a technology route for further increasing the density of silicon chips without having to resort to difficult isolation techniques (trench, LOCOS, etc.) and without having to give up the 5 volt supply option at 0.5 μm geometries and perhaps beyond. In fact, there are practically no isolation constraints until the devices get so small or close together that direct tunneling may occur.

On the negative side, however, is the high cost of SOI starting material, particularly silicon-on-sapphire (SOS) wafers, and the added cost of SOI processing. Consequently, as SOI technology develops further, its acceptance will increasingly depend on the balance achieved between the density and performance advantages it offers and the cost of deviating from standard (bulk silicon) processing.

To advance rad-hard device technology further, as well as help keep SOI/SOS technology in competition with bulk silicon technology, continued DoD support of this area will be necessary, aimed primarily at:

- Continuing the drive to smaller SOI geometries, maintaining competition with bulk silicon.
- Demonstrating the manufacturability of these device structures.

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[2]Ibid, p. B4

- Proving their reliability by demonstrating that there are no new unique failure mechanisms in SOI.

- Utilzing the capability of this technology to provide microelectronics which can operate in very-high-dose-rate environments.

- Assuring a domestic supply of qualified SOI materials.

- Utilizing the high voltage and isolation characteristics of SOI to permit integration of bipolar and CMOS devices on the same substrate and even allow fabrication of power (up to 5 kV) integrated circuits with monolithically co-integrated logic circuits.

Four SOI technologies are currently being pursued, each providing its own special set of characteristics:

- SOS (Silicon-On-Sapphire): Established as the most favored rad-hard technology. Relatively expensive, but offers new applications in available material.

- SIMOX (Separation by IMplantation of OXygen): Current preference of the SOI community. Versatile and adequate for CMOS and, potentially, for bipolar and BiCMOS.

- Bonded: Provides bulk-like microstructure and purity which may be needed for bipolar and advanced (closely spaced) devices.

- ZMR (Zone Melt Recrystallization)/LSE (Lateral Solid-phase Epitaxy): Low cost and appears to be acceptable for CMOS.

At this time, functionality has been demonstrated in all of these materials. Working CMOS devices have been built in SIMOX, ZMR and SOS structures, and bipolar devices have been built in bonded and SIMOX structures. For further significant progress to occur, however, a much better understanding of SOI materials and device structures will have to be achieved, particularly in regard to:

- Yield and reproducibility related to material properties,

- Properties adequate for higher-density circuits, and

- Specific requirements associated with various applications.

It should be noted that despite what seems to be a do-or-die competition among these four approaches, there is not likely to be an ultimate single "winner." Chances are that two or more of these materials will always be needed to satisfy different sets of requirements.

Reliability and Quality - System applications in DoD and NASA stress very long system life compared to commercial and scientific computing environments. This long system life requires extended component manufacturing life, careful documentation of design, and system use parameters to allow component retrofit to achieve form, fit, and functional transportability in systems and subsystems across multiple generations of component fabrication technologies, with minimal system impact. Use of design capture tools, modeling, foundry-independent design environments, and QML (Qualified Manufacturers List) acceptance in the design and foundry process all offer promise.

The objective of the QML program is to bring the semiconductor manufacturing procedures used for commercial and military products closer together. This is particularly important in the low-volume ASIC marketplace, which lacks the economy-of-scale advantages of large-quantity production runs. The QML program has been successful in bringing about the merger of commercial and military practices by stressing TQM (total quality management) and quality control principles. However, further work is needed to advance this approach and to bring about even more cost and time savings.

Technical studies addressing the trade-offs between in-line SPC (statistical process control) and device test and screening will help determine the adequacy and applicability of reduced burn-in and single-temperature final electrical testing. The feasibility of wafer-level burn-in and at-speed electrical testing needs to be explored. Improvements in the design process, such as new tools and simulators with reliability assessment and testability features, are needed for both the commercial and military marketplaces.

Critical issues related to developing a common qualification document for use in both communities are being addressed by the NASA/USAF Space Parts Working Group, DESC, JEDEC 13 and 14 committees and the NECQ, and this effort needs to continue. The QML program has the potential to provide reliable/quality microcircuits for the DoD in a cost- effective manner. However, various issues such as Class S qualification and rad-hard parts testing still must be resolved. Also, this method has yet to be widely embraced by the majority of military-semiconductor vendors; thus, the actual impact of this system is still unknown. By supporting these efforts, the DoD will be able to considerably hasten a full determination of the limits of applicability of the QML procedure and hopefully expand its use throughout the 1990s.

A final note: the "quality revolution" in silicon IC manufacturing, although initiated in Japan, was based on methods conceived in the U.S. Since quality in the U.S. and well as in Japan is now measured in defects per million units instead of per hundred units as was the case just one decade ago, it is clear the the U.S. IC industry now has a core capability in quality control that is on a par with Japan's.

Special Packaging - The evolutionary change from single-chip to multichip packages (MCPs) has begun. However, present packaging technologies limit clock speeds to the 50 MHz region within a MCP and to approximately 25 MHz on a PWB, with backplane signals again reduced by 50%.

With the success that has been achieved in device technologies, the operating speed of equipment and systems is no longer device limited but limited by the time constraints and electrical delays introduced by chip-to-chip or module-to-module interconnects. Concurrent with higher density packaging, problems associated with thermal management must be solved as an integral part of each packaging approach developed.

Advances will still be made in improving the performance of the individual chips, but a technology revolution is needed in the way chips are connected together to form systems. Speeds greater than 150 MHz are being sought. Integrated circuits will need to be interconnected in such a way that the packaging interconnection method does not degrade the high speed signal. This will require a high-density packaging approach such as chip-on-substrate and chip-on-board, multichip packaging, or hybrid wafer scale integration. Interconnect techniques will include thin film technology on substrates with matching coefficient of expansion, flip chip attachment techniques, tape automated bonding (TAB), and fiber optic interconnects. These techniques will permit greater than 50% coverage of a substrate/board with silicon chips.

The motivation for doing this is twofold. First, the higher packaging density will allow for more computing "horsepower" to be packaged in the same area. Even more important, however, is the ability to interconnect chips in such a way that they can operate at much higher clock speeds. These higher speeds will require computer modeling of the entire system design, from the chip interconnect to the interconnecting backplane. New high speed techniques for backplane interconnect will also be required. The significant increases in packaging density will lead to corresponding increases in thermal density, resulting in the need for significant improvements in cooling methods. For ultrahigh-density applications, stacked wafer (3-D) packaging will be used, further aggravating the thermal problem and, by its nature, introducing unique thermal problems.

In summary, the electronics industry is poised to make revolutionary advancements in the performance, size and weight, and cost reduction of electronic systems through improvement in packaging, interconnect, cooling and maintenance concepts at levels of integration beyond the chip level.

Standards and Specifications - The differences between DoD and commercial device technology in the area of standards and specifications are not the issue; of far more consequence are the differences between DoD applications and commercial applications. Whereas commercial technology is cost driven with reliability/quality concerns secondary, DoD devices are primarily reliability/quality driven, although the ultimate cost of achieving the level of reliability desired is also a concern. High performance is required by both DoD and commercial system designers.

Whether an application is civil or military, only those tests should be performed that are necessary to assure reliability. It is wasteful to maintain outdated testing requirements that address problems that no longer exist. To eliminate such outmoded requirements, it is critical that DoD reexamine its specifications and standards to determine which reliability screens add value and which are only cost drivers with little positive effect. For example, burn-in testing should be performed on new technologies and mature products to determine the time/temperature

requirements that assure reliability. If, however, it is shown that current microcircuits require reduced burn-in time, cost can be greatly reduced. (Present requirements are T_a = 125°C for 160 hours for Class B and Ta = 125°C for 240 hours for Class S, where T_a = ambient temperature.) A related example concerns the feasibility of performing reliability testing at wafer level for different silicon technologies.

New or modified methods for determining assembly process quality and reliability are required, especially for the new semiconductor materials and interconnect technologies being considered by designers. Reliability studies are required to determine if materials being proposed for military-grade microcircuits possess latent reliability problems that might appear in use. Such studies would also form the basis for eventual realization of a common set of silicon technology standards and specifications for both the DoD and commercial industry. These are examples of activities that would not only make industry more responsive to DoD needs, but benefit commercial products as well.

Assured Sources - The military market for semiconductors is about $2 billion per year; however, this expenditure level does not guarantee that all devices required for defense systems will be available. Because of the long time between system design and device procurement, some device types may be discontinued before the equipment is actually manufactured. Advancing microcircuit technology also causes problems related to the supplying of spares for fielded equipment—typically systems that have been in the field for upwards of 10 years with parts 20 to 30 years old.

Semi-custom or custom designs are not immune to obsolescence. For example, the life cycle of a gate array is typically seven years, but can be as brief as seven months. Not only are the changes in microcircuit availability quite rapid, the costs associated with the use of obsolete parts are significant. The 1991 Report on Diminishing Manufacturing Sources and Material Shortages submitted to the Deputy Assistant Secretary of Defense (Logistics) by the Joint Logistics Commanders predicts that over the next two to five years the cost of redesigns required to correct microcircuit nonavailability problems will exceed $2.9 billion.

Among the several approaches taken to reduce the cost impact of parts obsolescence are: stockpiling, acquisition of discontinued product stock, microcircuit emulation, and use of the VHSIC Hardware Description Language (VHDL) to capture digital designs at both the device and board level in order to be able to replicate in new technology the form, fit and function of an earlier device that may no longer be available.

Of the techniques used to ensure cost-effective availability of obsolete parts, some are proactive and others are reactive. The best approach requires consideration of many factors.

The Microelectronics Technology Support Program (MTSP) at SM-ALC has two primary objectives. The first is to develop form, fit and function emulation replacements for electronic components rapidly and includes analysis, design, simulation, fabrication, postprocessing and packaging, prototyping, testing and limited production of custom microcircuits, boards,

subsystems, and systems. Functionally dense state-of-the-art semiconductors can replace not only older integrated circuits but older circuit boards as well. Combinations of them can replace subsystems and sometimes systems. The MTSP is not a "normal" spares procurement contract. Therefore, the procurement of spares directly from existing reprocurement data is outside the scope of the statement of work. However, it is appropriate to analyze, reverse engineer, design, develop and prototype spares up to and including limited production.

The second objective calls for accelerating the operational use of advanced technologies by overcoming traditional impediments. The approach involves developing insertions and applications of advanced technologies to support weapon system reliability and maintainability requirements. The aim is to demonstrate the capability of, or evaluate the supportability of, these advanced technologies. This includes evaluating the feasibility of insertions, prototyping and integrating insertions and evaluating the impact on test equipment, reliability, testability, packaging, and systems. The contract requires application of existing advanced technologies to DoD problems. Examples are VHSIC, MIMIC and certain electro-optic devices.

The MTSP provides DoD with a flexible, quick-reaction capability by providing rapid access to technology experts. The MTSP source selection included three sample tasks designed to test each offeror's technical capability: (1) reverse engineering of an integrated circuit, (2) a PCB redesign, and (3) a PCB redesign targeted for single chip (high functional density) replacement.

Rapid Prototyping - Two major efforts supported by DoD in the area of flexible manufacturing are the Microelectronics Manufacturing Science and Technology (MMST) program and Generalized Emulation of Microcircuits (GEM) program. Their objectives are to develop and implement flexible manufacturing methodologies that will permit the rapid and affordable acquisition of advanced integrated circuits for military systems by the mid-1990s and beyond. The efforts address eight major areas:

1. process development;
2. standard common modular processing systems;
3. *in-situ* sensors;
4. real time process control;
5. computer integrated manufacturing (CIM) for overall factory control, scheduling, recipe downloading, and automatic report generation;
6. facility/technology demonstrations;
7. vendor interactions and/or co-developments; and
8. technology transfer.

Specific goals are:

1. a throughput of 800 six-inch wafers/month;
2. 0.35 micrometer minimum feature size;
3. a minimum turnaround time of three days;
4. facility size of < 2500 ft^2; and
5. total facility cost of < $30M.

Both the MMST and GEM programs emphasize silicon but are equally applicable to GaAs microwave and digital devices, HgCdTe focal plane detector arrays, and other types of semiconductor devices produced in small quantities for military applications. Both programs lead the industry in the development of advanced CIM software for semiconductor manufacturing. Generic equipment models and detailed reports on this CIM software have been supplied to SEMATECH. In fact, the programs are closely coordinated with the work at SEMATECH—specifically to complement SEMATECH's development of high-volume, commercial production technology and equipment.

The MMST and GEM technologies are particularly applicable to the production of low-volume, high-complexity semiconductor devices for special military applications, such as: radiation-hardened devices for space applications, highly secure devices, custom-designed ASICs for individual systems, and replacement of parts that are no longer manufactured. In addition, some commercial semiconductor manufacturers are finding that this new approach is also applicable to high-volume 16MB DRAM production, which involves high-cost, large wafers.

Process development has concentrated on 0.35 micrometer, 3.3 volt CMOS, selected as the demonstration vehicle for the next generation of technology. Experiments have shown that CMOS devices are faster than BiCMOS devices at those design-rule levels in addition to being much less complex and therefore more economical to process. Working silicon devices have been obtained using rapid thermal processing in MMST standard modular equipment. A set of *in-situ* sensors has been developed for these modules to permit real-time process control, implemented on 68030 machines in SMALLTALK. The CIM system is also being implemented in SMALLTALK for factory control, scheduling, and reporting. This new object-oriented language is being adopted by SEMATECH. The first Modular Processing System (MPS) has been completed and installed in the MMST fab facility. Lithography has been successful down to 0.35 micrometer with a Canon DUV stepper. As part of the GEM program, VHDL descriptions of the GEM library will be linked to behavioral synthesis tools and direct-write e-beam lithography.

Appendix E

LIST OF ACRONYMS

AGED	ADVISORY GROUP ON ELECTRON DEVICES
ANN	ARTIFICIAL NEURAL NETWORK
ASIC	APPLICATION SPECIFIC INTEGRATED CIRCUIT
ASUW	ANTI-SURFACE WARFARE
ASW	ANTI-SUBMARINE WARFARE
BiCMOS	BIPOLAR/COMPLEMENTARY METAL OXIDE SEMICONDUCTOR
BIST	BUILT-IN SELF TEST
C^3I	COMMAND, CONTROL, COMMUNICATIONS, INTELLIGENCE
CAD	COMPUTER-AIDED DESIGN
CCD	CHARGE COUPLED DEVICE
CIM	COMPUTER INTEGRATED MANUFACTURING
CM	COUNTERMEASURES
CMOS	COMPLEMENTARY METAL OXIDE SEMICONDUCTOR
DARPA	DEFENCE ADVANCED RESEARCH PROJECTS AGENCY
DDR&E	DEPUTY DIRECTOR, RESEARCH & ENGINEERING
DESC	DEFENSE ELECTRONICS SUPPLY CENTER
DNA	DEFENSE NUCLEAR AGENCY
DRAM	DYNAMIC RANDOM ACCESS MEMORY
DUV	DEEP ULTRAVIOLET
ECCN	EXPORT CONTROL COMMODITY NUMBER
ECM	ELECTRONIC COUNTERMEASURES
ELINT	ELECTRONIC INTELLIGENCE
EW	ELECTRONIC WARFARE
FET	FIELD EFFECT TRANSISTOR
FLOPS	FLOATING POINT OPERATIONS PER SECOND
FPA	FOCAL PLANE ARRAY
GEM	GENERALIZED EMULATION OF MICROCIRCUITS
GFLOPS	BILLIONS OF FLOATING POINT OPERATIONS PER SECOND
GoCo	GOVERNMENT-OWNED, CONTRACTOR-OPERATED
GPS	GLOBAL POSITIONING SATELLITE
IC	INTEGRATED CIRCUIT
IR	INFRARED
JDL	JOINT DIRECTORS OF LABORATORIES
JEDEC	JOINT ELECTRON DEVICE ENGINEERING COUNCIL
LOCOS	LOCAL OXIDATION OF SILICON
LSE	LATERAL SOLID-PHASE EPITAXY
MCC	MICROELECTRONICS AND COMPUTER (TECHNOLOGY) CORP.
MCM	MULTICHIP MODULE
MCNC	MICROELECTRONICS CENTER OF NORTH CAROLINA
MCP	MULTICHIP PACKAGE
MCTL	MILITARY CRITICAL TECHNOLOGIES LIST
MFLOPS	MILLIONS OF FLOATING POINT OPERATIONS PER SECOND

MIMIC	MICROWAVE/MILLIMETER-WAVE MONOLITHIC INTEGRATED CIRCUIT
MMC	MASSACHUSETTS MICROELECTRONICS CENTER
MMIC	MICROWAVE MONOLITHIC INTEGRATED CIRCUIT
MMST	MICROELECTRONICS MANUFACTURING SCIENCE AND TECHNOLOGY
MOSFET	METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR
MPS	MODULAR PROCESSING SYSTEM
MTSP	MICROELECTRONICS TECHNOLOGY SUPPORT PROGRAM
NECQ	NATIONAL ELECTRONIC COMPONENT QUALITY (ASSESSMENT SYSTEM)
NSA	NATIONAL SECURITY AGENCY
NVM	NONVOLATILE MEMORY
PCB	PRINTED CIRCUIT BOARD
PWB	PRINTED WIRING BOARD
QML	QUALIFIED MANUFACTURERS LIST
RECCE	RECONNAISSANCE
SAR	SYNTHETIC APERTURE RADAR
SIMOX	SEPARATION BY IMPLANATION OF OXYGEN
SM-ALC	SACRAMENTO-AIR FORCE LOGISTICS CENTER
SOI	SILICON ON INSULATOR
SOS	SILICON ON SAPPHIRE
SP	SIGNAL PROCESSING/PROCESSOR
SPC	STATISTICAL PROCESS CONTROL
SRAM	STATIC RANDOM ACCESS MEMORY
SRC	SEMICONDUCTOR RESEARCH CORPORATION
STAR	SPECIAL TECHNOLOGY AREA REVIEW
TAB	TAPE AUTOMATED BONDING
TCAD	TECHNOLOGY COMPUTER-AIDED DESIGN
TOW	TUBE-LAUNCHED, OPTICALLY TRACKED, WIRE-GUIDED ANTITANK MISSILE
TPED	PROJECT RELIANCE/TRI-SERVICE TECHNOLOGY PANEL FOR ELECTRONIC DEVICES
TQM	TOTAL QUALITY MANAGEMENT
VHDL	VHSIC HARDWARE DESCRIPTION LANGUAGE
VHSIC	VERY HIGH SPEED INTEGRATED CIRCUIT
VLSI	VERY LARGE SCALE INTEGRATION
ZMR	ZONE MELT RECRYSTALLIZATION